ABSTRACT OF THE DISCLOSURE

A memory subsystem includes a memory controller coupled to a memory module including a plurality of memory chips via a memory bus. The memory controller may

5 generate a plurality of memory requests each including address information and corresponding error detection information. The corresponding error detection information is dependent upon said address information. The memory module may receive each of the plurality of memory requests. An error detection circuit within the memory module may detect an error the address information based upon the

10 corresponding error detection information and may provide an error indication in response to detecting the error.